CLAIMS:

1. A modeling process comprising:

providing a plurality of blocks, each of the blocks representing functional entities that operate on a plurality of input signal values;

generating a plurality of output signal values from the plurality of blocks;

grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

outputting the first composite signal.

2. The process of claim 1 wherein each of the blocks includes at least one input signal port and at least one output signal port.

3. The process of claim 1 wherein the input signal values and the output signal values have at least one attribute.

4. The process of claim 3 wherein the attribute is a name.

5. The process of claim 3 wherein the attribute is a data type.

6. The process of claim 3 wherein the attribute is a numeric type.

7. The process of claim 3 wherein the attribute is a dimensionality.

8. The process of claim 1 wherein the ordered set is a linked list data structure.

9. The process of claim 8 wherein the linked list data structure is a tree data structure, the tree data structure including m + n nodes.

10. The process of claim 9 wherein m represents a number of independent signals and n represents a number of composite signals.

11. The process of claim 1 further comprising decomposing the first composite signal into the plurality of output signals in a demultiplexer.

12. The process of claim 1 further comprising viewing the ordered set contained in the first composite signal with a composite signal viewer.

13. The process of claim 1 wherein at least one of the input signal values is a second composite signal.

14. A block diagram modeling process comprising:

providing a first block and a second block, the blocks representing functional entities that operate on a plurality of input signal values;

generating a plurality of output signal values from the first and second block;

grouping the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

processing the composite signal in a third block.

15. The process of claim 14 wherein the ordered set is a linked list data structure.

16. The process of claim 14 wherein at least one of the input signals is a second composite signal.

17. The process of claim 14 further comprising decomposing the composite signal into the plurality of input signal values.

18. The process of claim 14 further comprising viewing the composite signal in a composite signal viewer.

19. The process of claim 18 wherein the composite signal viewer displays the ordered set contained in the composite signal on a graphical user interface (GUI).

20. The process of claim 19 wherein the GUI is provided on an input/output device.

21. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

provide a plurality of blocks, each of the blocks representing functional entities that operate on a plurality of input signal values;

generate a plurality of output signal values from the plurality of blocks;

group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

output the first composite signal.

22. The computer program product of claim 21 wherein the computer readable medium is a random access memory (RAM).

23. The computer program product of claim 21 wherein the computer readable medium is read only memory (ROM).

24. The computer program product of claim 21 wherein the computer readable medium is hard disk drive.

25. A processor and a memory configured to:

provide a plurality of blocks, each of the blocks representing functional entities that operate on a plurality of input signal values;

generate a plurality of output signal values from the plurality of blocks;

group the plurality of output signal values as an ordered set in a multiplexer as a first composite signal; and

output the first composite signal.

26. The processor and memory of claim 25 wherein the processor and the memory are incorporated into a personal computer.

27. The processor and memory of claim 25 wherein the processor and the memory are incorporated into a network server residing in the Internet.

28. The processor and memory of claim 25 wherein the processor and the memory are incorporated into a single board computer.

29. A modeling process comprising:

providing a plurality of blocks, each of the blocks representing a functional entity that operates on one or more input signal values and generates one or more output signals;

grouping the output signals use an ordered set in a multiplexer as a composite signal; and

outputting the composite signal.

30. The process of claim 29 wherein the ordered set is a tree data structure.

31. The process of claim 30 wherein the tree data structure is a linked list.

32. The process of claim 29 further comprising:

providing a composite signal viewer; and

viewing the ordered set in a graphical user interface executing in the composite signal viewer.

33. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to:

provide a plurality of blocks, each of the blocks representing a functional entity that operates on one or more

input signal values and generates one or more output signal values;

group the output signals as an ordered set in a multiplexer as a composite signal; and

output the composite signal.

34. A processor and memory configured to

provide a plurality of blocks, each of the blocks representing a functional entity that operates on one or more input signal values and generates one or more output signal values;

group the output signals as an ordered set in a multiplexer as a composite signal; and

output the composite signal.